REMARKS

In section 2 of the Office Action, the Examiner rejected claims 1, 8-12, 21, and 22 under 35 U.S.C. §103(a) as being unpatentable over the Yu patent. Claims 1, 8-12, 21, and 22 are cancelled.

The Yu patent shows in Figure 1 a trellis having four states and five sections. For convenience, the Yu patent references M states per trellis section and N trellis sections per block or frame. A maximum *a posterior* (MAP) decoder implements forward and backward generalized Viterbi recursions or soft output Viterbi algorithms (SOVA) up to a present section. The past and future bit probabilities are used along with the present branch metric to generate an output bit decision.

A baseband communication system is depicted in Figure 2 of the Yu patent, where the information sequence b_k is turbo encoded, is mapped to 1 or -1 transmitted symbols s_i, is passed through a channel interleaver π_c, and is transmitted over an intersymbol interference (ISI) channel.

At a receiver, the received signal y_i is based on the transmitted symbols s_i, noise n_i, and the channel impulse response h_j, which increases the likelihood of bit

errors when a receiver attempts to decode the signal to obtain the original information bits b_k. According to the Yu patent, turbo encoding and decoding minimizes bit errors due to the noise n_i, but not intersymbol interference (ISI).

Figure 3 of the Yu patent shows the turbo encoder of the transmitter. The turbo encoder employs one interleaver π and two recursive systematic convolutional codes (RSC1 and RSC2). The output c_k of the turbo encoder is generated by concatenating the information bits b_k at the input of the turbo encoder with the parity bits p_{1k} and p_{2k} produced by the turbo encoder.

Figure 4 shows a turbo decoder 150 that employs an interleaver π, de-interleavers π^{-1}, and decoders DEC1 and DEC2, and that is useful in decoding a signal x_k that includes noise n_i. Assuming zero decoder delay, the first decoder DEC1 computes a soft output L_{e1k} from the received information bits x_k^s, from the received first parity bits x_k^{p1}, and from feedback L_{ak} derived from the second decoder DEC2.

The second decoder DEC2 is provided with an interleaved version of the soft output L_{e1k}, with a de-interleaved version of the received information bits x_k^s, and with the received second parity bits x_k^{p2}. The second

decoder DEC2 generates extrinsic information L_{e2k}, which is deinterleaved to produce the feedback L_{ak}. After a predetermined number of iterations, a de-interleaved soft output $\hat{b}_k$ is generated as an estimate of the original information bits b_k. A slicer is included in the decoders DEC1 and DEC2 to make hard decisions about the original information bits b_k.

According to the Yu patent, the decoder of Figure 4 is effective with the noise n_i, but not with intersymbol interference (ISI) due to the channel impulse response.

Figure 5 shows a turbo decoder with a decision feedback equalizer (DFE) that provides intersymbol interference equalization in decoding a received turbo coded input signal. Specifically, an decision feedback equalizer loop 160 has been added to the turbo decoder 150 of Figure 4 in order to deal with intersymbol interference (ISI).

The turbo decoder 150 decodes the information bits and the parity bits of the input signal, and calculates soft output values for the information bits and parity bits of the input signal as described above. Typically, the soft output values are log-likelihood ratio (LLR) values.

The decision feedback equalizer loop 160 is coupled to the turbo decoder 150 to receive hard decision values for the information and parity bits. The decision feedback equalizer loop 160 includes a decision feedback equalizer 100 that processes the hard decision on each symbol along with updated estimates of channel characteristics derived from the previous frame to calculate an intersymbol interference correction signal. As shown in Figure 6, the decision feedback equalizer 100 is a typical decision feedback equalizer filter.

Equalization is implemented in an iterative process. The decision feedback signal provided by the decision feedback equalizer 100 applies a channel correction signal $\tilde{y}_i$ to the next input of the signal before the signal is input to the turbo decoder 150, thereby minimizing the intersymbol interference (ISI). That is, the channel correction signal $\tilde{y}_i$ provided by the decision feedback equalizer 100 is subtracted from the received distorted signal y_i to produce the input signal x_i corrupted only by the noise n_i.

The decision feedback equalizer 100 is initialized with all zero values in the first iteration. The input signal x_i is deinterleaved (π_c^{-1}) and is demultiplexed to separately output the received

information bits x_k^s and the received parity bits x_k^{p1} and x_k^{p2}. The received information bits x_k^s and the received parity bits x_k^{p1} and x_k^{p2} are applied to the recursive decoders DEC1 and DEC2 as described above.

After the first iteration, the log-likelihood ratio (LLR) values of the received information bits and the received parity bits are calculated. These log-likelihood ratio (LLR) values are then sliced by a slicer of the turbo decoder in order to make the information bit hard decisions $\hat{b}_k$ and the parity bit hard decisions $\hat{p}_{1k}$ and $\hat{p}_{2k}$. The information bit hard decisions $\hat{b}_k$ and the parity bit hard decisions $\hat{p}_{1k}$ and $\hat{p}_{2k}$ are multiplexed and mapped to the estimated channel symbols $\hat{s}_i$.

The estimated channel symbols $\hat{s}_i$ are channel interleaved at π_c and are fed into the decision feedback equalizer 100. The decision feedback equalizer 100 applies the channel impulse response h_j to the estimated channel symbols $\hat{s}_i$ to produce the channel correction signal $\tilde{y}_i$. The channel correction signal $\tilde{y}_i$ is subtracted from the received signal y_i as shown in Figure 5 to produce the input signal x_i. Although the estimated symbols $\hat{s}_i$ may not all be correct, the symbol error

probability decreases as the number of iterations increases due to large turbo coding gain and to the decision feedback equalizer loop 160.

Because the channel may change over time, the channel impulse response h_j is updated to track the changes in the channel. The least mean squared (LMS) error algorithm, for example, can be used to update the channel impulse response h_j based on a predetermined step size Δ and an equalization error ε.

Newly added independent claim 43 is directed to a method for providing enhanced slice prediction comprising receiving an input containing first and second data, decoding the input with a first decoder to recover both the first and second data, decoding only the second data with a second decoder, and providing enhanced slice prediction based on the decoding of the second data. Each data element of the first data represents a number of bits that is greater than a number of bits represented by each data element of the second data, and the first and second data in the received input are defined by the same n level constellation.

The Yu patent does not disclose or suggest a first decoder that decodes an input to recover both first

and second data and a second decoder that decodes only the second data.

The Examiner may consider the decoder DEC1 to correspond to the first decoder recited in independent claim 43 and the decoder DEC2 to correspond to the second decoder recited in independent claim 43. Then, assuming that the first and second data of independent claim 43 are the received information bits x_k^s and the received parity bits x_k^{p1}, the decoder DEC1 decodes the first and second data to produce an output L_{e1k}. The decoder DEC2, however, decodes the output L_{e1k}, which is a function of both the first and second data and not just the second data. Therefore, the apparatus disclosed in the Yu patent does not disclose or suggest a first decoder that decodes an input to recover both first and second data and a second decoder that decodes only the second data as required by independent claim 43.

Therefore, independent claim 43 is not unpatentable over the Yu patent.

Because independent claim 43 is not unpatentable over the Yu patent, dependent claims 44-63 are likewise not unpatentable over the Yu patent.

CONCLUSION

In view of the above, it is clear that the claims of the present application are patentable over the art applied by the Examiner. Accordingly, allowance of these claims and issuance of the above captioned patent application are respectfully requested.

Respectfully submitted,

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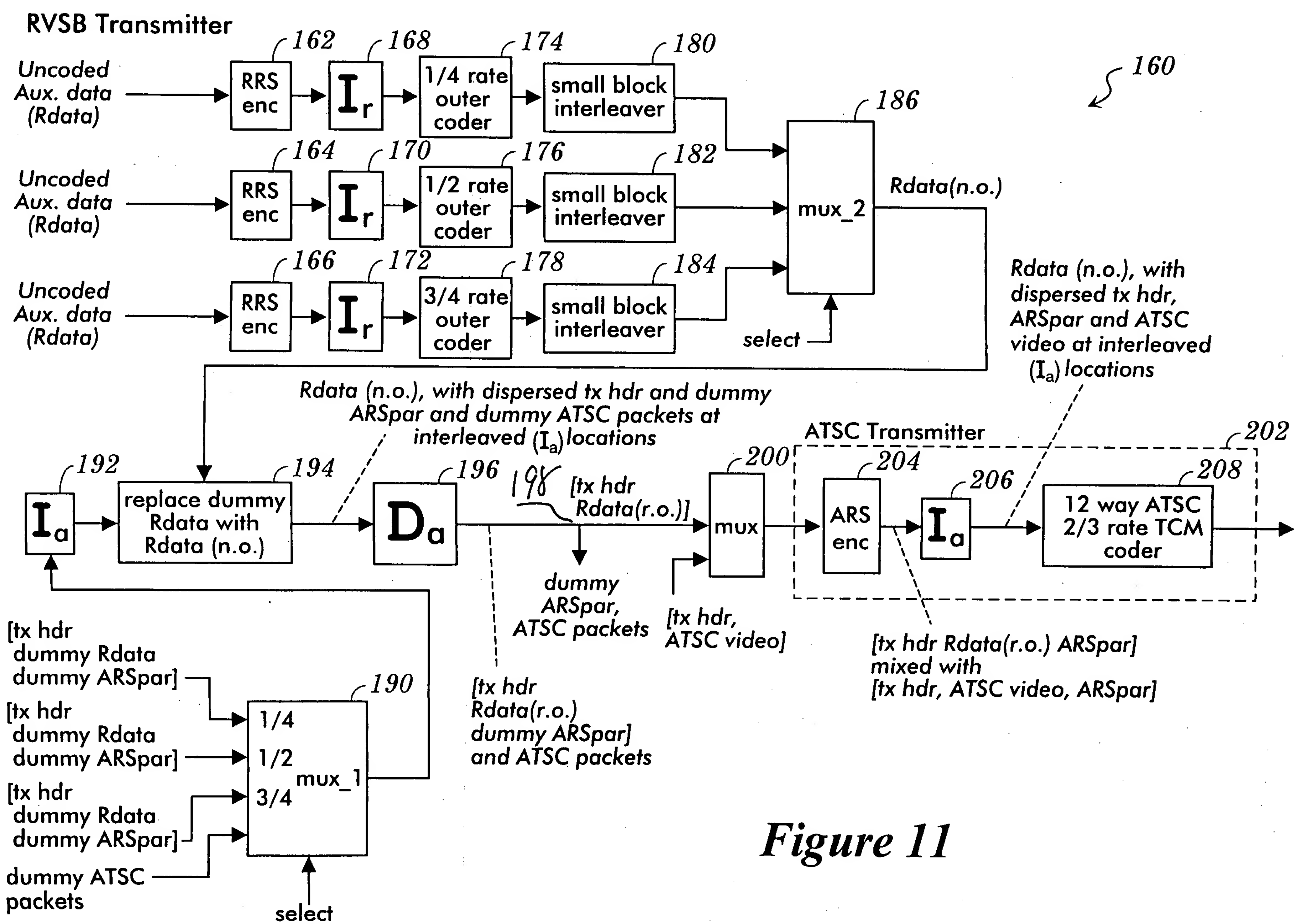
January 14, 2005

IN THE DRAWINGS

With the concurrence of the Examiner, the drawings are amended to add the reference numeral 198 to Figure 11 as shown by the red ink notation on the accompanying copy of Figure 11. Amended formal drawings are being contemporaneously submitted.



RVSB Transmitter
160
Uncoded Aux. data (Rdata)
Uncoded Aux. data (Rdata)
Uncoded Aux. data (Rdata)
162
RRS enc
164
RRS enc
166
RRS enc
168
I_r
170
I_r
172
I_r
174
1/4 rate outer coder
176
1/2 rate outer coder
178
3/4 rate outer coder
180
small block interleaver
182
small block interleaver
184
small block interleaver
186
mux_2
select
Rdata(n.o.)
Rdata (n.o.), with dispersed tx hdr, ARSpar and ATSC video at interleaved (I_a) locations
192
I_a
194
replace dummy Rdata with Rdata (n.o.)
Rdata (n.o.), with dispersed tx hdr and dummy ARSpar and dummy ATSC packets at interleaved (I_a) locations
196
D_a
198
[tx hdr Rdata(r.o.)]
dummy ARSpar, ATSC packets
[tx hdr Rdata(r.o.) dummy ARSpar] and ATSC packets
200
mux
[tx hdr, ATSC video]
ATSC Transmitter
202
204
ARS enc
206
I_a
208
12 way ATSC 2/3 rate TCM coder
[tx hdr Rdata(r.o.) ARSpar] mixed with [tx hdr, ATSC video, ARSpar]
[tx hdr dummy Rdata dummy ARSpar]
[tx hdr dummy Rdata dummy ARSpar]
[tx hdr dummy Rdata dummy ARSpar]
dummy ATSC packets
190
1/4
1/2
3/4
mux_1
select

Figure 11